WHAT IS CLAIMED IS:

1. A digital signal delay compensating circuit:

a first semiconductor circuit device including a clock-signal generating circuit and a data processing circuit for outputting a data signal in synchronism with a clock signal generated by the click-signal generating circuit; and

a second semiconductor circuit device to which the data signal output from the first semiconductor circuit device is inputted and which processes the data signal in synchronism with the clock signal,

wherein the clock signal to be supplied from the first semiconductor circuit device to the second semiconductor circuit device is fed back to the data processing circuit, and the fed-back clock signal is used as a clock signal at the time of outputting the data signal.

2. The signal delay compensating circuit according to claim 1, wherein the clock signal is fed back from a clock signal input terminal of the second semiconductor circuit device to the data processing circuit.

3. The signal delay compensating circuit according to claim 1, wherein the clock signal is fed back from a clock signal output terminal inside the first semiconductor circuit device to the data processing circuit.

4. A digital signal delay compensating circuit comprising:

a storage device capable of writing data therein; and

a semiconductor circuit device including an access timing signal generating circuit for writing the data in the storage device and adapted to write the data in the storage data,

wherein an access timing signal to be supplied from the semiconductor circuit device to the storage device is fed back to the semiconductor circuit device, and a reference signal for allowing the semiconductor circuit device to output data to be written in the storage device is made active in a case where both the fed-back signal and a signal outputted from the access timing signal generating circuit are active.